Micro- and Nano-Electronics Group

Research Annual Report - 2008

1) **DESIGN OF RF INTEGRATED CIRCUITS**
L. Larcher, A. Mazzanti, M. Borgarino, R. Brama, F.Ducati, F.Chiesi, D.Dermit, A.Ricciardi, G.Manni, M. Ganzerli
Collaborations: ST-Microelectronics, NXP, Entropic, Politech'Nice, Univ. Pavia, Univ. Pisa, Univ. Parma, Univ. Perugia.
Area: Integrated Circuits and Systems

2) **COMPOUND-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS FOR RF POWER APPLICATIONS**
A. Chini, F. Fantini, M. Faqir, G. Verzellesi
Collaborations: Selex S.I. (Roma), Slovak Academy of Science, Bratislava (Slovakia), Thales (France), Univ. Padova, Politecnico di Torino, Univ. Roma Tor Vergata, Univ. Bologna (Dipart. Fisica).
Area: Microelectronic and Nanoelectronic Devices

3) **CHARACTERIZATION AND MODELING OF NON VOLATILE MEMORY CELLS**
P. Pavan, L. Larcher, A. Padovani, G. Betti Beneventi
Collaborations: Univ. Padova, Univ. Ferrara, Univ. "La Sapienza" Roma, Politecnico di Milano, IU.net, ST-Microelectronics, Saifun Semiconductors Ltd.
Area: Microelectronic and Nanoelectronic Devices

4) **RADIATION DETECTORS ON 4H-SIC AND HIGH-RESISTIVITY SI**
F. Nava, G. Verzellesi
Collaborations: INFN, Selex S.I., FBK Trento, CNR-IMM, Ioffe Institute, IKZ Berlin, Politecnico di Milano, Univ. Bologna, Univ. Trento, Univ. Trieste, Univ. Pisa, Univ. Firenze, Univ. Perugia, Univ. Torino, Univ. Milano-Bicocca, Univ. Catania.
Area: Sensors, Microsystems and Instrumentation

5) **DESIGN OF ENERGY SCAVENGING CIRCUITS**
L. Larcher, A. Bertacchini, D. Dondi, P. Pavan
Collaborations: ST-Microelectronics, Univ. Bologna.
Area: Power Electronics and Industrial Applications

6) **RELIABILITY OF ELECTRONIC SYSTEMS**
F. Fantini, G. Cassanelli, M. Faqir
Collaborations: Spal spa, Prof. M. Vanzi (DIEE Cagliari).
Area: Electronic Systems and Applications

DESIGN OF RF INTEGRATED CIRCUITS

L. Larcher, A. Mazzanti, M. Borgarino, R. Brama, M. Pifferi, F.Ducati, F.Chiesi, M. Ganzerli

Area: Integrated Circuits and Systems

The activity on RF design of Silicon integrated circuits covers several research projects. We focused on the analysis and design of wireless transceivers for communications and sensors applications. We investigated low power and innovative circuit techniques for RF front-ends, frequency sysnthesis and power amplifiers. Several test chips (Class-E power amplifiers, injection locked oscillators, LNAs, mixers, PLLs, X-band radiometer) have been designed and succesfully tested. In particular a monolithic radiometer working in X-band has been succesfully tested with electrical characterisations and electromagnetic tests, as well. We investigated also effects of high-voltage device stresses on oxide breakdown at Radio Frequency. Presently the attention is focused on CMOS design of building blocks for Ultra Wide Band and millimeter-wave transceivers, Clock and Data Recovery circuits for S-ATA, SSH and Fiber Channel standards, and CATV. In collaboration with the Politechnic of Nice (France), several enabling building blocks for Ku-band communication applications have been design in 120nm CMOS and tested.

Publications

[1] R. Brama, L. Larcher, A. Mazzanti, and F. Svelto, "30.5dBm 48 % PAE CMOS Class-E PA with integrated balun for RF Applications", IEEE Journal of Solid-State Circuits, Vol. 43, no. 8, pp. 1755-1762, 2008

[2] F.Ducati, M.Pifferi, M.Borgarino, "Self-oscillation Free 0.35um Si/SiGe BiCMOS X-Band Digital Frequency Divider", IEEE Microwave and Wireless Components Letters, vol. 18, no. 7, 2008, pp. 473-475

[3] M.Pifferi , F.Ducati, H.Brekelmans, L.Tripodi, M.Borgarino, K.Doris, "A Broadband RF 65nm CMOS Front-End for cable TV reception", Microelectronics Journal, vol. 39, issue 5, 2008, pp. 703-710

[4] F.Chiesi, M.Borgarino, A.Mazzanti, E.Sacchi, G.Albasini, W.Audoglio, "65nm CMOS SSB mixer for UWB synthesizer", International Journal of Electronic, vol. 95, no. 4, 2008, pp. 305-312

[5] F.Ducati, A.Mazzanti, M.Borgarino, M.Pifferi, "SiGe BiCMOS X-Band Integrated Radiometer", IEEE International Conference on Electronics, Circuits and Systems, 2008, pp. 1257-1260

[6] F.Alimenti, D.Zito, A.Boni, M.Borgarino, A.Fonte, A.Carboni, S.Leone, M.Pifferi, L.Roselli, B.Neri, R.Menozzi, "System-on-Chip Microwave Radiometer for Thermal Remote Sensing and its Application to the Forest Fire Detection", IEEE International Conference on Electronics, Circuits and Systems, 2008, pp. 1265-1268

[7] M.Pifferi, M.Borgarino, "High linearity BiCMOS I-Q demodulator", SAME2008 Conference (Sophia Antipolis, France)

[8] F.Ducati, F.Chiesi, D.Dermit, G.Manni, P.Lucchi, F.B.Abdeljelil, F.Sala, M.Borgarino, G.Jacquemod, "Ku-Band PLL functional blocks", SAME2008 Conference (Sophia Antipolis, France)

[9] F.Ducati, F.Chiesi, N.Corciulo, M.Borgarino, G.Jacquemod, "Ku-Band receiver functional blocks", SAME2008 Conference (Sophia Antipolis, France).

[10] A. Mazzanti, E. Sacchi, P. Andreani, and F. Svelto, "Analysis and Design of a Double-Quadrature CMOS VCO for Subharmonic Mixing at Ka-Band", IEEE Transactions on Microwave Theory and Techniques, Vol. 56, no. 2, pp. 355-363, 2008.

[11] L.Lu, Z.Tang, P.Andreani, A.Mazzanti, and A.Hajimiri, "Comments on A General Theory of Phase Noise in Electrical Oscillators", IEEE Journal of Solid State Circuits, Vol.43 no.9, pp.2170, 2008.

[12] A.Mazzanti and P.Andreani, "Class C Harmonic CMOS VCOs, with a General Result on Phase Noise", IEEE Journal of Solid State Circuits, Vol.43 no.12, pp.2716-2729, 2008.

[13] A.Mazzanti, M.Sosio, M.Repossi, and F.Svelto, "A 24GHz Sub-Harmonic Receiver Front-End with Integrated Multi-Phase LO Generation in 65nm CMOS", IEEE International Solid State Circuit Conference (ISSCC), pp.216,217,608 San Francisco, Feb. 2008.

[14] A.Mazzanti and P.Andreani, "A 1.4mW 4.90-to-5.65GHz Class C CMOS VCO with an Average FoM of 194.5dBc/Hz", IEEE International Solid State Circuit Conference (ISSCC), pp. 474,475,629, San Francisco, Feb. 2008.

[15] S. Bozzola, D.Guermandi, A.Mazzanti, and F.Svelto, "An 11.5IEEE Radio Frequency Integrated Circuits (RFIC) Symposium 2008, pp.657-660, Atlanta, June 2008.

[16] F.Vecchi, M.Repossi, A.Mazzanti, P.Arcioni, and F.Svelto "A Simple and Complete Circuit Model for the Coupling Between Symmetrical spiral Inductors in silicon RFICs", IEEE Radio Frequency Integrated Circuits (RFIC) Symposium 2008, pp.479-482, Atlanta, June 2008.

COMPOUND-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS FOR RF POWER APPLICATIONS

A. Chini, F. Fantini, M. Faqir, G. Verzellesi

Area: Microelectronic and Nanoelectronic Devices

This research activity addresses the development, characterization, numerical simulation, and reliability assessment of GaAs- and GaN-based field-effect transistors for RF power applications. Specific results published in 2008 can be summarized as follows.

(i) State-of-the-art Field-Plated GaAs-based pHEMTs have been fabricated and tested by means of pulsed I-V, DLTS and RF Power measurements [1,2]. The effect of field-plate length on DC and RF operation of pHEMTs has been analyzed showing that the adoption of an optimal fieldplate structure can significantly boost the device RF power performance, resulting in power density up to 2W/mm measured under continuous wave RF signals at 2GHz. The physical origin of the DC-to-RF dispersion in the fabricated devices has also been associated with a hole-trap located at 0.65eV from the valence band as obtained from current-DLTS measurements. The experimental results have been also supported and validated by numerical simulations. Numerical simulations

highlighet that the beneficial effects arising from the adoption of the field-plate structure lie in its control on the trapped charge population responsible for the DC to RF dispersion mechanism.

(ii) High-electric-field degradation phenomena have been investigated in GaN-capped AlGaN-GaN HEMTs by comparing experimental data with numerical device simulations [3]. 150-hour DC stresses were carried out under power-state and off-state conditions. Degradations effects characterizing both stress experiments were: a drop in the DC drain current, the amplification of gate-lag effects, and a decrease in the reverse gate leakage current. Numerical simulations indicate that the simultaneous generation of surface (and/or barrier) traps and of buffer traps can account for all of the above degradation modes. Experiments showed also that the power-state stress induced a drop in the transconductance at high gate-source voltages only, whereas the off-state stress led to a uniform transconductance drop over the entire gate-source-voltage range. This behavior can be reproduced by simulations provided that, under power-state stress, traps are assumed to accumulate over a wide region extending laterally from the gate edge towards the drain contact, whereas, under off-state stress, trap generation is supposed to take place in a narrower portion of the drain access region close to the gate edge and to be accompanied by a significant degradation of the channel transport parameters.

(iii) Failure modes and mechanisms of AlGaN/GaN HEMTs, observed during accelerated tests at various bias conditions, have been reviewed [4]. Extensive testing of various GaN technologies has demonstrated that the increase of the density of deep levels is the dominant failure mechanism of AlGaN/GaN HEMTs. For the tested submicron devices, trap generation can be ascribed to hot carriers only at moderate drain bias (i.e., less than 20 V). At higher drain voltages, more complex mechanisms play a role, involving inverse piezoelectric effects and localized hot carrier injection from the gate, thus enhancing degradation effects. Suitable device structures adopting field plates, gate insulator layers and/or recessed gate active areas are therefore required in order to control these effects.

(iv) The physical mechanisms underlying RF current collapse effects in passivated AlGaN-GaN HEMTs have been investigated by means of measurements and numerical device simulations [5,6]. Our study suggests that 1) both surface and buffer traps can contribute to RF current collapse through a similar physical mechanism involving capture and emission of electrons tunneling from the gate; 2) surface passivation strongly mitigates RF current collapse by reducing the surface electric field and inhibiting electron injection into traps; 3) for surface-trap densities lower than 9×10^{12} cm^{-2}, surface potential barriers in the 1-2 eV range can coexist with surface traps having much a shallower energy and therefore inducing RF current collapse effects characterized by relatively-short time constants.

(v) Electrical characterizations and reliability analysis have been performed on AlGaN/GaN HEMTs processed on epitaxial layers grown on composite substrates [7]. The results showed that this tecnology is very promising for the fabrication of low cost high power microwave transistors for wireless communication systems. The excellent characteristics of the fabricated devices have also been highlighted by their RF power performances. Power densities up to 4 W/mm have been measured at 2 GHz. The experimentally obtained data confirm that the layer transfer based composite substrates are very promising for high performance low-cost RF GaN HEMT structures for power applications.

(vi) The influence of self-heating effects on current-mode DLTS measurements on GaN HEMTs has been studied [8]. It has been shown that device self-heating can significantly influence the

extraction of trap ionization energy leading to a large underestimation of the latter. Ionization energies as low as 80meV and non-overlapping Arrhenius plots are obtained when device self-heating are neglected. On the other hand, when thermal effects are taken into account by correcting the measured data, an ionization energy of approximately 200meV was extracted and a reasonable overlap of the Arrhenius plots is obtained by measurement carried out at different drain-source biases.

Publications

[1] A. Chini, M. Esposto, G. Verzellesi, S. Lavanga, C. Lanzieri, A. Cetronio, "Characterization and Numerical Simulations of High Power Field-Plated pHEMTs", Proc. of the European Microwave Integrated Circuits Conference (EuMIC 2008), pp. 218-221, Amsterdam (The Netherlands), Oct. 2008.

[2] A. Chini, V. di Lecce, M. Esposto, G. Verzellesi, S. Lavanga, A. Cetronio, C. Lanzieri, "Trapping phenomena in field-plated high power GaAs pHEMTs", Proc. of the 17th European Workshop on Heterostructure Technology (HeTech08), pp. 65-66, Venezia (Italy), Nov. 2008.

[3] M. Faqir, G. Verzellesi, G. Meneghesso, E. Zanoni, F. Fantini, "Investigation of High-Electric-Field Degradation Effects in AlGaN/GaN HEMTs", IEEE Transactions on Electron Devices, vol. 55(7), pp. 1592-1602, July 2008.

[4] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, E. Zanoni, "Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives", IEEE Transactions on Device and Materials Reliability, vol. 8(2), pp. 332-343, June 2008.

[5] M. Faqir, G. Verzellesi, A. Chini, F. Fantini, F. Danesin, G. Meneghesso, E. Zanoni, C. Dua, "Mechanisms of RF Current Collapse in AlGaNGaN High Electron Mobility Transistors", IEEE Transactions on Device and Materials Reliability, vol. 8(2), pp. 240-247, June 2008.

[6] M. Faqir, G. Verzellesi, A. Chini, F. Fantini, F. Danesin, F. Rampazzo, G. Meneghesso, E. Zanoni, N. Labat, A. Touboul, C. Dua, "Effects of surface and buffer traps in passivated AlGaN/GaN HEMTs", Proc. of the 32th Workshop On Compound Semiconductor Devices and Integrated Circuits (WOCSDICE 2008), Leuven (Belgium), May 2008, pp. 111-112.

[7] F. Zanon, F. Danesin, A. Tazzoli, M. Meneghini, N. Ronchi, A. Chini, P. Bove, R. Langer, E. Zanoni, and G. Meneghesso, "Reliability aspects of GaN-HEMTs on composite substrates", ASDAM 2008, The Seventh International Conference on Advanced Semiconductor Devices and Microsystems, October 12-16, 2008, Smolenice Castle, Slovakia

[8] A. Chini, M. Esposto, M. Bonaiuti, G. Verzellesi, F. Zanon, E. Zanoni, G. Meneghesso, "Influence of Device Self-Heating on the Activation Energy Extraction During Current-DLTS Measurement", Proc. of the 17th European Workshop on Heterostructure Technology (HeTech08), pp. 49-50, Venezia (Italy), Nov. 2008.

CHARACTERIZATION AND MODELING OF NON VOLATILE MEMORY CELLS

P. Pavan, L. Larcher, A. Padovani, G. Betti Beneventi

Area: Microelectronic and Nanoelectronic Devices

We have continued the research activity concerning the characterization and the modeling of traditional and emerging non-volatile memories. Specifically, the research activity we carried out has been focused on investigating high-k material used in NVM field and TANOS memories.

Publications

[1] L. Larcher, A. Padovani, P. Pavan, P. Fantini, A.Calderoni, A. Mauri and A. Benvenuti, "Modeling NAND Flash memories for IC design", IEEE Electron Device Letters, Vol. 29(10), pp. 1152 1154, 2008

[2] A. Padovani, L. Larcher, S. Verma, P. Pavan, P. Majhi, P. Kapur, K. Parat, G. Bersuker, K. Saraswat, "Statistical modeling of leakage currents through SiO2/high-k dielectric stacks for non-volatile memory applications", IEEE International Reliability Physics Symposium (IRPS), 2008, pp. 616-620

[3] Padovani, A.; Larcher, L.; Verma, S.; Pavan, P.; Majhi, P.; Kapur, P.; Parat, K.; Bersuker, G.; Saraswat, K, "Feasibility of SIO2/Al2O3 tunnel dielectric for future Flash memories generations", Ultimate Integration of Silicon (ULIS), 2008, pp. 111-114

[4] G. Puzzilli, F. Irrera, P. Pavan, L. Larcher, A. Arya, A. Pirovano, "On the RESET-SET Transition in Phase Change Memories", Proc. of ESSDERC, pp. 158-161, 2008

[5] P. Fantini, G. Betti Beneventi, A. Calderoni, L. Larcher, P. Pavan and F. Pellizzer, "Characterization and Modeling of Low-Frequency Noise in PCM device", IEEE-IEDM, San Francisco (CA), pp. 219-222, 2008

[6] G. Bersuker, D. Heh, C. Young, H. Park, P. Khanal, L. Larcher, A. Padovani, P. Lenahan, J. Ryan, B. H. Lee, H. Tseng, R. Jammy, "Breakdown in the metal/high-k gate stack: identifying weak link in the multilayer dielectric", IEEE-IEDM, San Francisco (CA), pp. 791-794, 2008

RADIATION DETECTORS ON SIC AND HIGH-RESISTIVITY SI

F. Nava, G. Verzellesi, L. Rovati, M. Bonaiuti

Area: Sensors, Microsystems and Instrumentation

This research activity is aimed at the development of ionizing radiation detectors on 4H-SiC and high-resistivity Si for scientific and industrial applications.
Results achieved on 4H-SiC detectors are the following:

(i) the electrical and optical characterization of Schottky barrier diodes realized in different geometries (circular dot , pixel, interdigital contact, microstrips, etc.) on 4H-SiC epitaxial layers with thickness and dopant concentration of 150 μm and 3x10^{13} cm^{-3}, respectively. The undoped n-type 4H-SiC epitaxial layer is grown at the Epitaxial Technology Center of Catania, Italy, using a hot wall Chemical Vapor Deposition reactor by LPE S.p.a. of Milano, Italy. Beta spectroscopy measurements are in progress with the main purpose to demonstrate that with so high thickness and low dopant concentration a good signal to noise ratio detection is possible also at high temperature (90 C), where detectors, realized on stndard material such as Si, GaAs and CdTe, do not work [1] .

(ii) the responsivity measurements of Schottky barrier diodes used as UV photodetectors as a function of the wavelength ranging from 200 to 400 nm and the study of the effect of induced defects by 1 MeV neutron irradiation at different fluences on the responsivity. Preliminar results [2] show that at fluences equal or higher than 8x10^{14} n/cm^2, the rejection rate is in the order of 103 in the range 200-320 nm while it is less than 102 at about 320 nm. Measurements of the responsivity are in progress by using 4H-SiC Schottky diodes with interdigit contacts as a function of 1 MeV neutron irradiation at fluences ranging from 10^{13} to 10^{16} n/cm^2. The measurements are performed in vertical as well in planar electrical configuration.

The activity on Si detectors has led to the development of a simple, low-cost, and low-power alpha-particle detection system for environmental radioactivity monitoring [3]. Alpha-particle detectors are of great interest for environmental radioactivity measurements, like Radon-concentration measurements for both health protection and volcanic- and seismic-activity monitoring. For these applications, the development of simple, low-cost, and low-power-consumption, alphaa-particle detection systems would significantly advance the state-of-the-art, enabling the deployment of battery-operated, portable instruments and detector networks. The proposed system exploits a previuosly-developed high-resistivity-silicon detector with internal amplification capability based on the bipolar-transistor (BJT) effect and readout electronics based on commercial ICs. Two-dimensional numerical device simulations have been adopted to assess the feasibility of the BJT detector as an alpha-particle detector that can be operated, without losing its internal signal amplification capability, with floating base and low collector voltages, so that device technology can be kept simple, very small DC power consumption can be achieved, and a single 5-V power-supply voltage can be used for readout electronics and detector biasing. The charge amplification accomplished by the BJT detector allows a single, commercial chip to be adopted, to perform charge preamplification and 20-bit A/D conversion. The digital output is sent to a low-cost microcontroller that can be periodically interrogated through the IR port. The cost of the readout electronics is in the order of 60 USD and it can operate with standard Li-ion battery for about 60 hours.

Publications

[1] F.Nava, G.Bertuccio, A.Cavallini, E.Vittone, "Silicon carbide and its use as a radiation detector material", Topical Review in Meas. Sci. and Technology 19 (2008), 10200 (25pp).

[2] A.Cavallini, A.Castaldini, F.Nava, "On the UV Responsivity of neutron irradiated 4H-SiC", Appl. Phys. Letters 93 (2008), 153502.

[3] L. Rovati, G. Verzellesi, M. Bonaiuti, G. Batignani, L. Bosisio, G.-F. Dalla Betta, G. Giacomini, C. Piemonte, N. Zorzi, "Radon alpha-ray detector based on a high-resistivity-silicon BJT and a low-cost readout electronics", Proc. of 2008 IEEE International Instrumentation and Measurement

Technology Conference (I2MTC 2008), pp. 1403-1406, Victoria, Vancouver Island (Canada), May 2008.

DESIGN OF ENERGY SCAVENGING CIRCUITS

L. Larcher, A. Bertacchini, D. Dondi, P. Pavan

Area: Power Electronics and Industrial Applications

The development of perpetually powered systems avoiding periodical battery replacement and/or recharge is one of the ultimate goals in sensor network design. In fact, even if advances in low-power design can help extending battery lifetime, the amount of the energy provided by storage devices still constrains the autonomy of distributed embedded systems such as Wireless Sensor Networks (WSN). The research activity is focused on the design of high efficiency scavenging circuits for ultra low power applications. These circuits are able to harvest energy from several renewable source like solar light, piezoelectric materials, thermal gradients, RF, etc. The application field of these circuits is not limited to self powered WSN nodes, but it can be easily extended also in embedded portable applications to extend battery life. In particular we investigated several circuit architecture for small-size photovoltaic scavengers and for RF harvesters (preliminary studies). Compared to large-scale PhotoVoltaic (PV) systems, small-size photovoltaic scavengers have to deal with the following issues: (a) the energy budget is small due to the size of the cells; (b) implementation of efficient Maximum Power Point (MPP) circuits usually takes large part of the power harnessed; (c) there is a substantial interaction between scavenger and the powered devices. This leads to the consideration that the design phase must be supported by simulations, in particular when conversion efficiency has to be optimized when solar irradiance is low. The definition of a clear design flow is fundamental to develop circuit solutions with optimized efficiency and better performances. This requires circuit simulations of the complete solar harvester system, which have been proposed for large-scale PV systems, but are highly desirable also for low power harvester circuits for wireless sensor networks. To obtain representative simulations, accurate models should be developed. Therefore, the validation of an accurate compact model of the non-linear I-V characteristics of PV modules is essential to design efficient harvester systems. In this scenario, we studied a high-efficiency ultra low-power MPP tracking circuit for environmentally powered wireless sensor network nodes. A compact model of the PV module based on a simplified parameter extraction procedure , allowing reproducing its I-V characteristics without numerical approaches has been developed. This model predicts the instantaneous power collected by the panel helping the harvester design and optimization procedure. Moreover, a detailed modelling of the harvester has been investigated to understand basic harvester behavior and optimize the circuit. Consequently, we have also studied a methodology for optimizing a solar harvester with maximum-power point tracking for self powered wireless sensors networks (WSN) nodes. We focus on maximizing the harvesters efficiency in transferring energy from the solar panel to the energy storing device.

Publications

[1] A. Bertacchini, D. Dondi, L. Larcher, and P. Pavan, "Performance Analysis of Solar Energy Harvesting Circuits for Autonomous Sensors", IEEE IECON, Orlando (FL), pp. 2655-2660, 2008

[2] D. Dondi, A. Bertacchini, L. Larcher, P. Pavan, D. Brunelli and L. Benini, "A Solar Energy Harvesting Circuit for Low Power Applications", IEEE ICSET, Singapore, pp. 945-949, 2008

[3] D. Dondi, A. Bertacchini, L. Larcher, L. Benini, D. Brunelli, "Modeling and Optimization of a Solar Energy Harvester System for Self Powered Wireless Sensor Networks", IEEE Trans. on Industrial Electronics, Vol. 55, no. 7, pp. 2759 2766, 2008

[4] D. Brunelli, D. Dondi, A. Bertacchini, L. Larcher, L. Benini, P. Pavan, "Photovoltaic scavenging system: modeling and optimization", Microeletronics Journal, 2008

RELIABILITY OF ELECTRONIC SYSTEMS

F. Fantini, G. Cassanelli, M. Faqir

Area: Electronic Systems and Applications

Aim of this activity is the development of reliability methodologies that can be used to evaluate and to improve the reliability of electronics systems during the early design phase. Failure analysis techniques for advanced devices have been developed, in particular for GaN LEDs.

Publications

[1] G.Mura, G.Cassanelli, F.Fantini, M.Vanzi, "Sulfur-contamination of high power white LED", Microelectronics Reliability, 48,1208-1211, 2008.